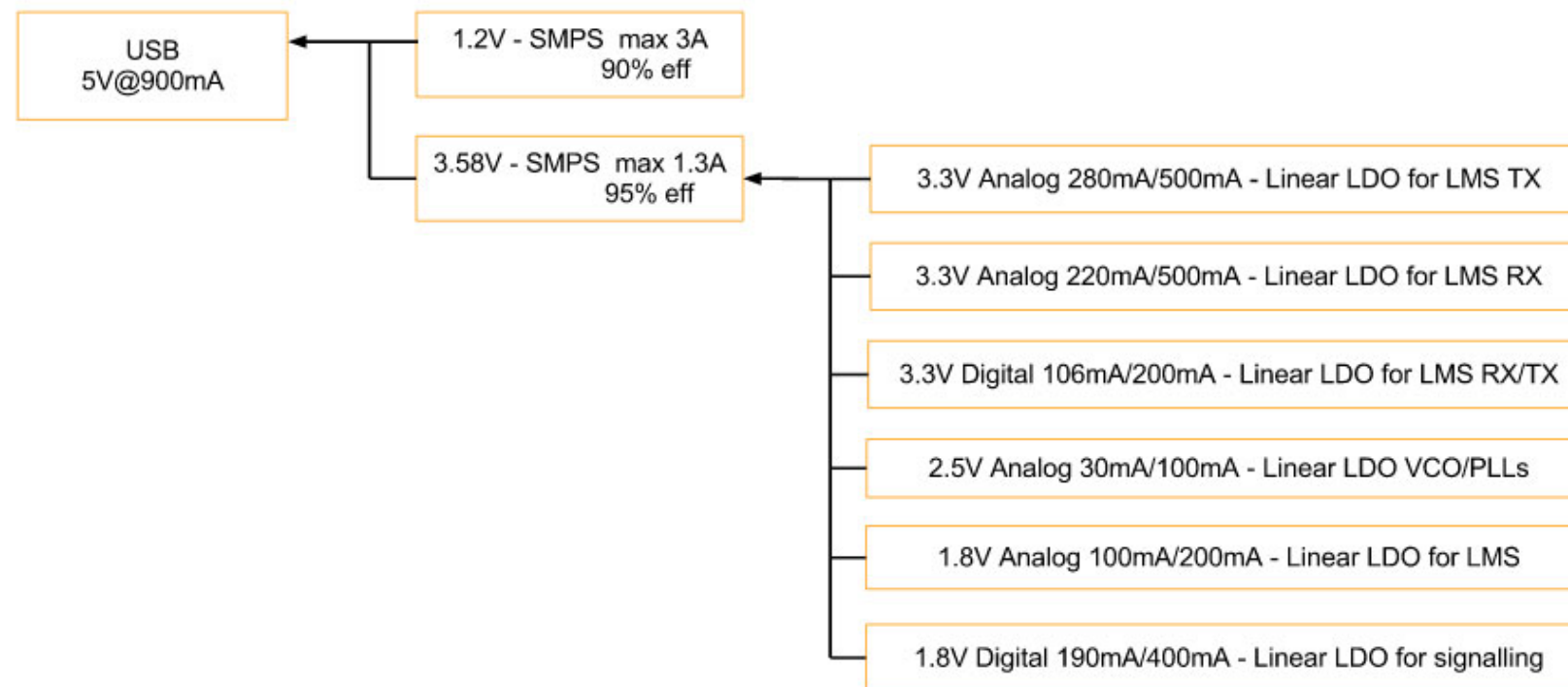
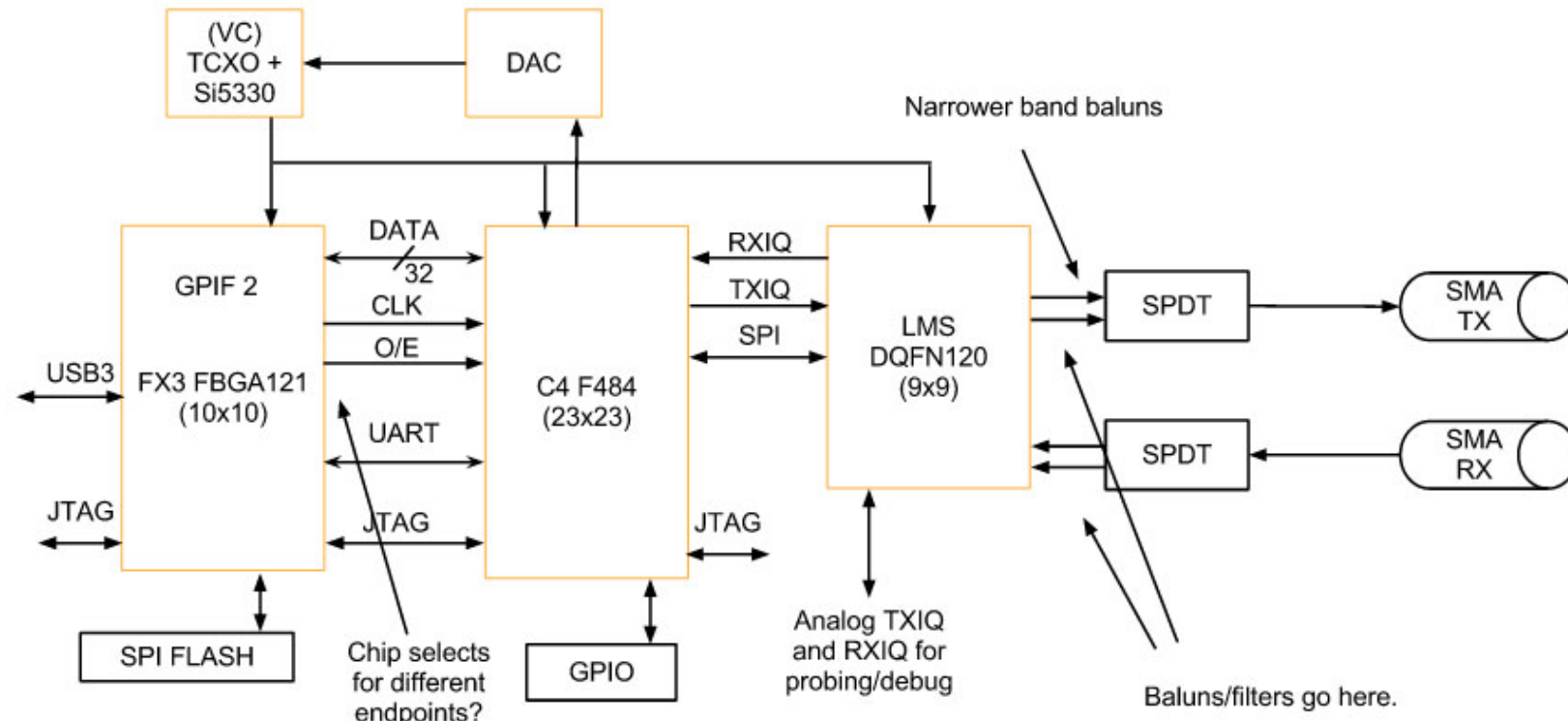
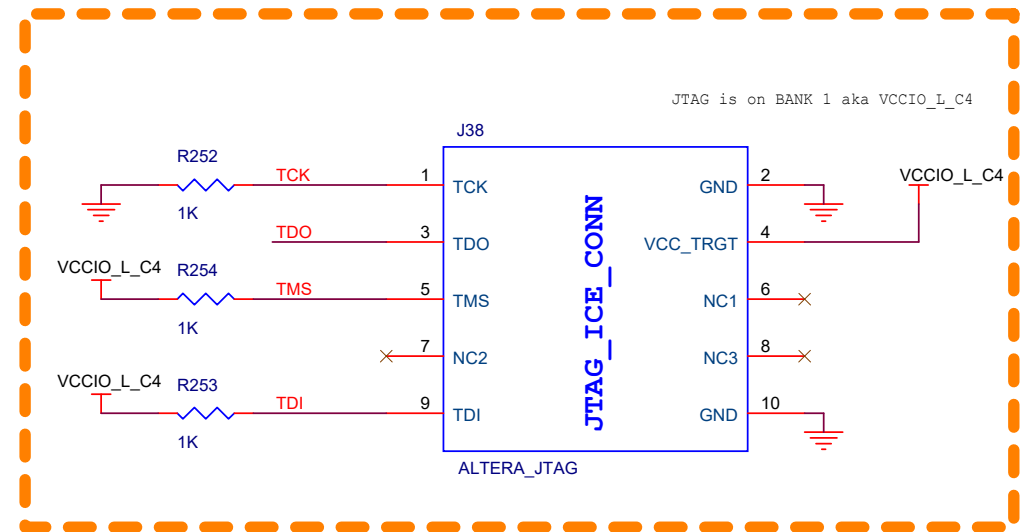
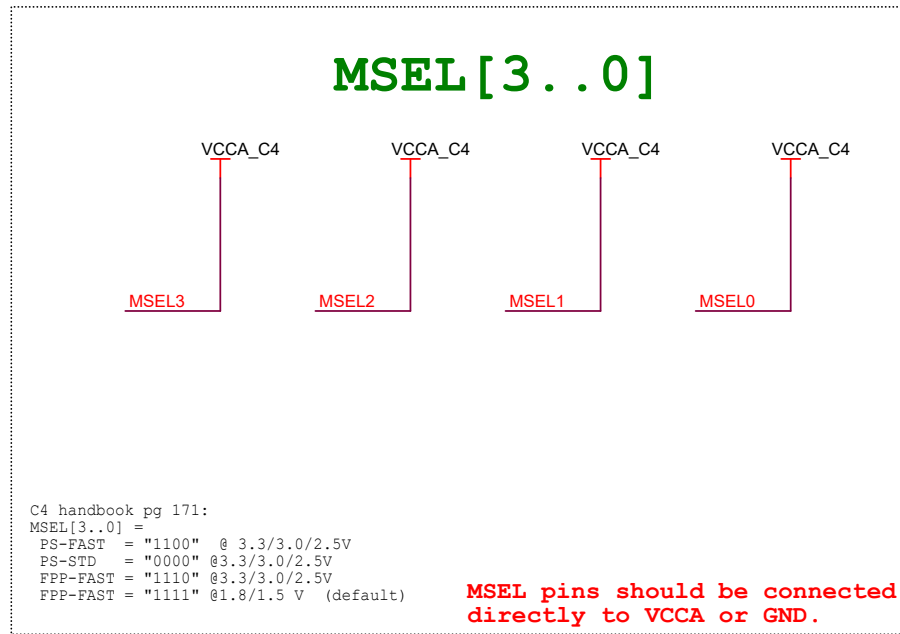
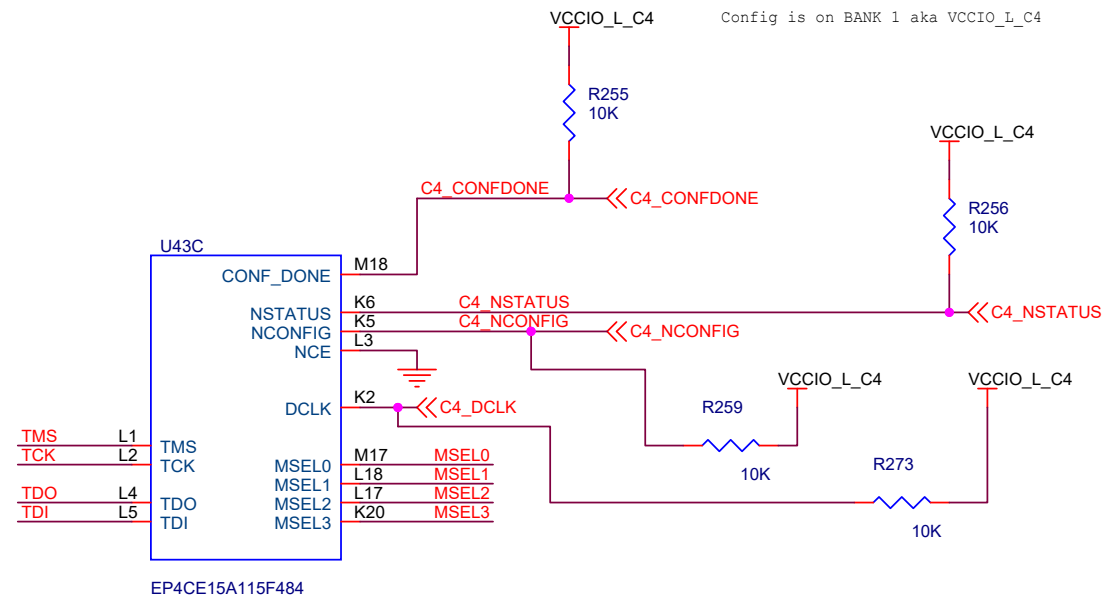


bladerRF - USB 3.0 Software Defined Radio



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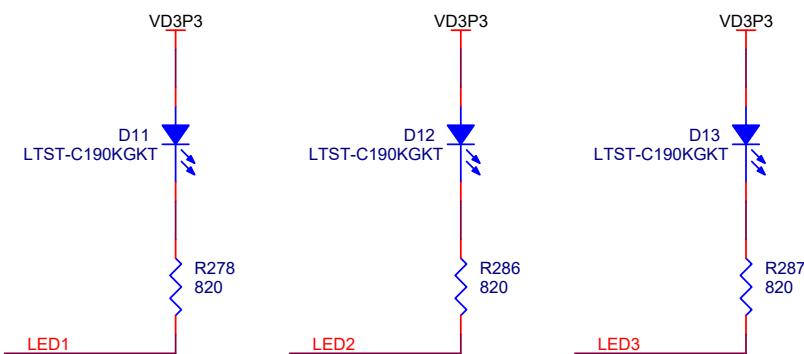
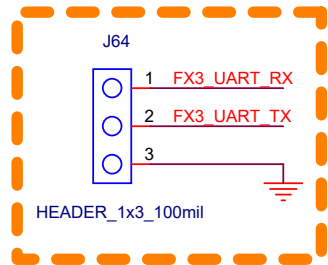
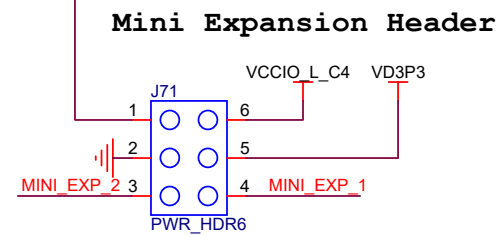
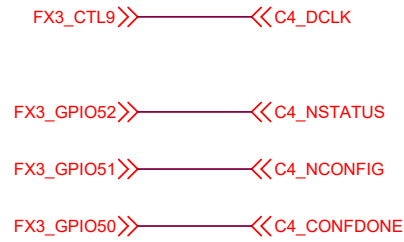
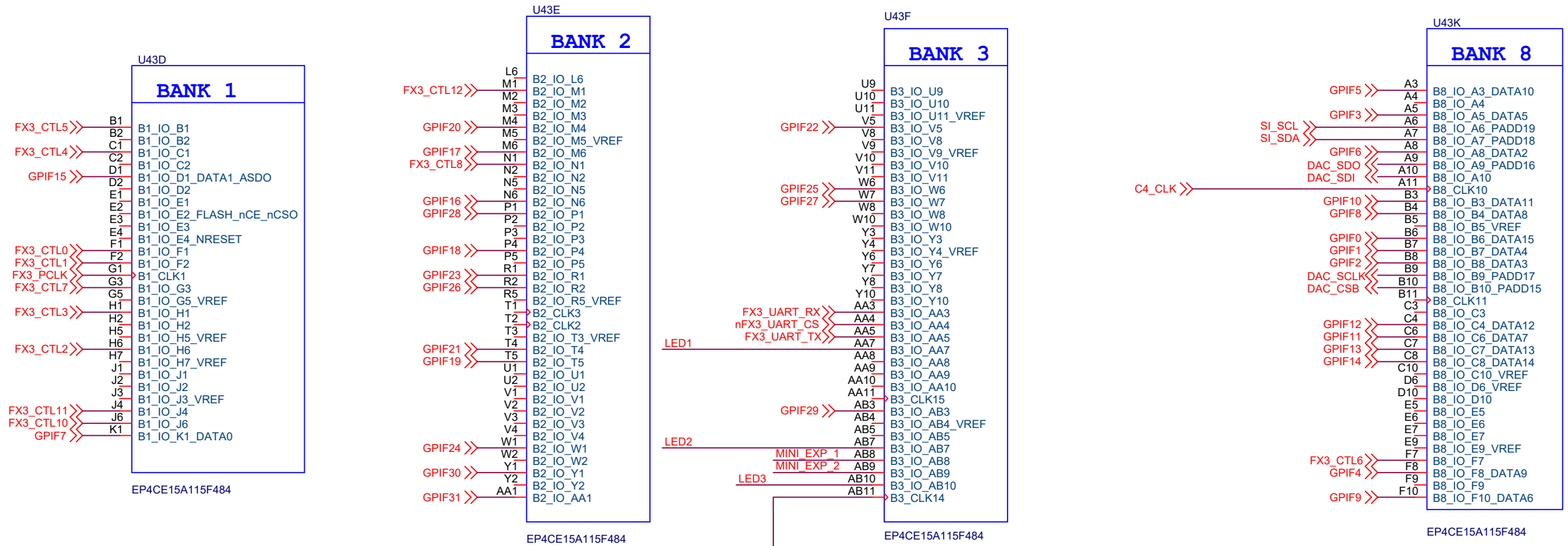
FPGA CONFIGURATION



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Avoid VREF pins due to their slow IO times.
 UDCLK has to be a CTL pin.
 DATA[0..7] have to be from GPIF[0..15]

FPGA "LEFT" BANK

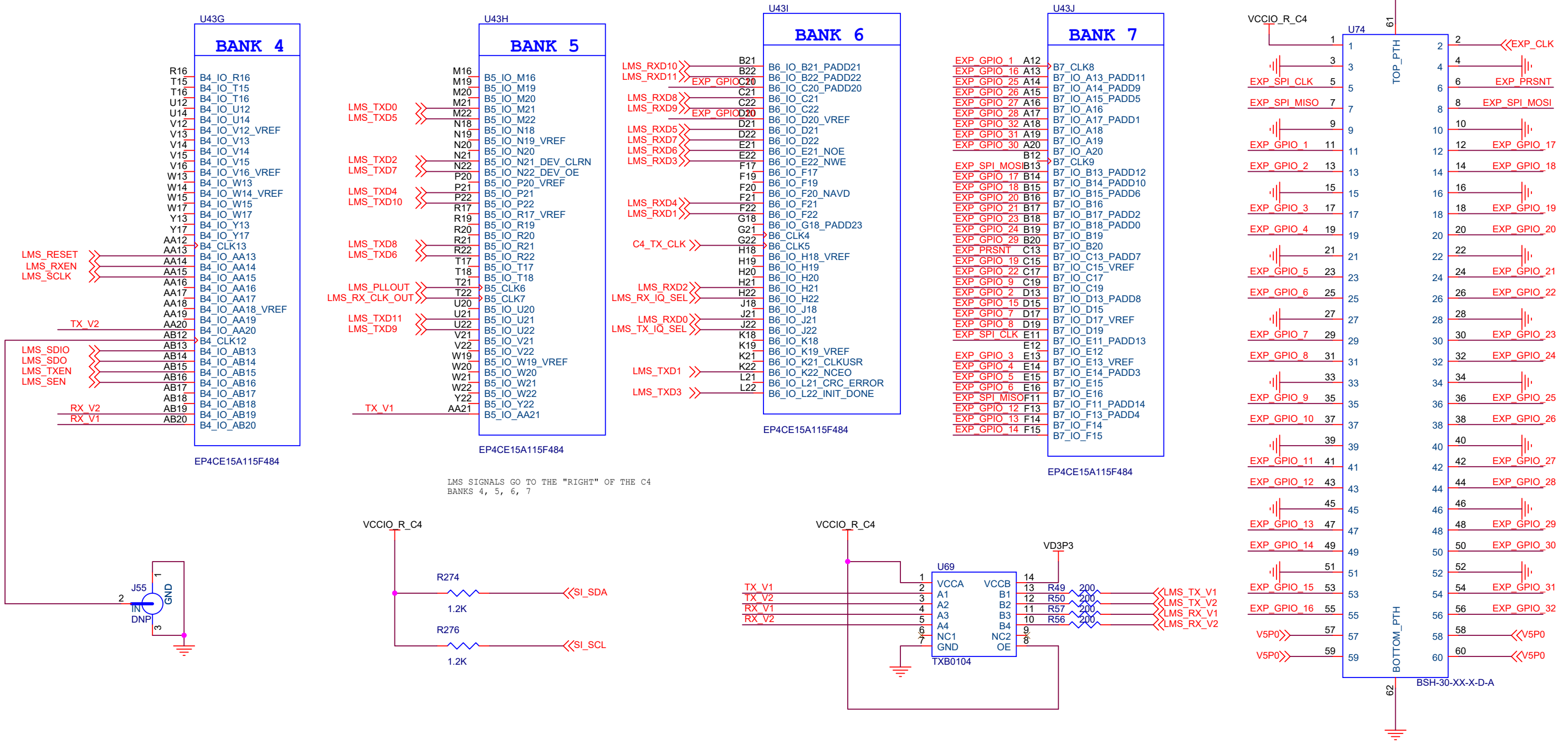


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FPGA "RIGHT" BANK

Avoid VREF pins due to their slow IO times.

Expansion Header

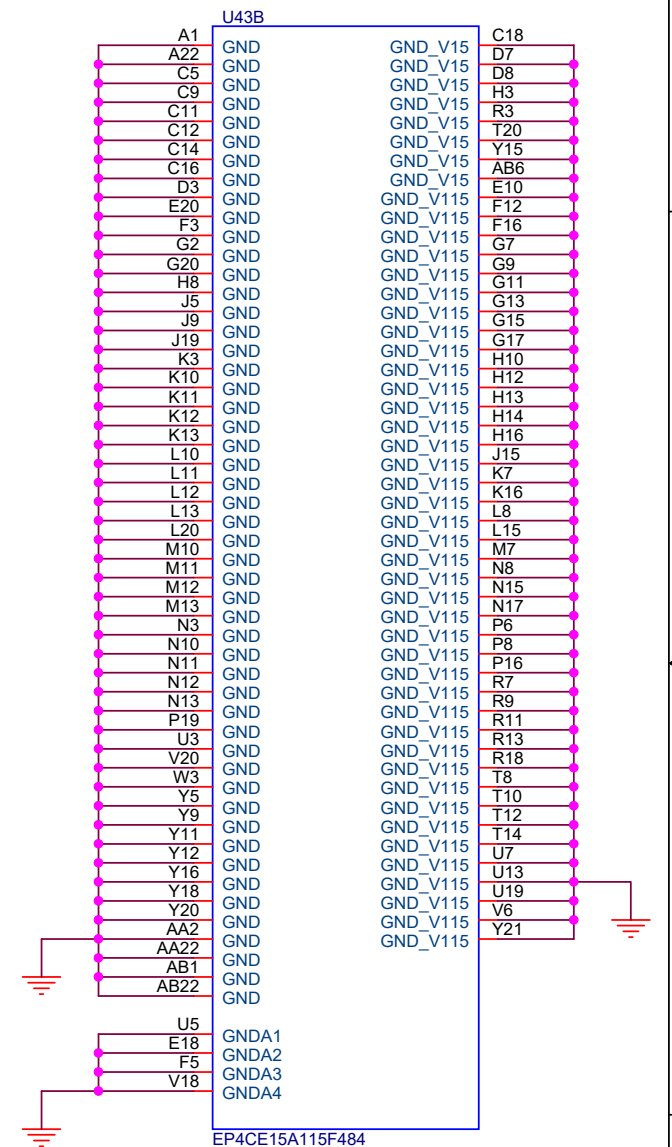
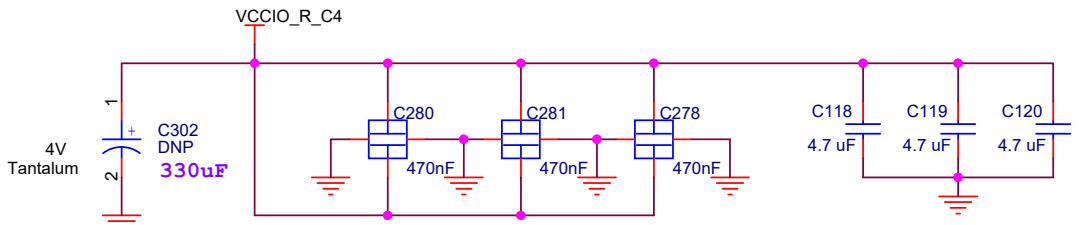
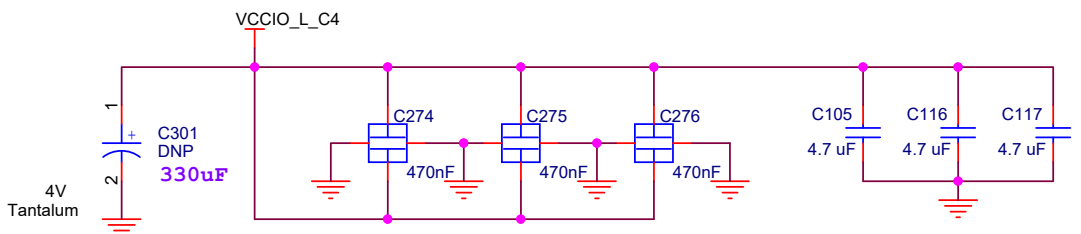
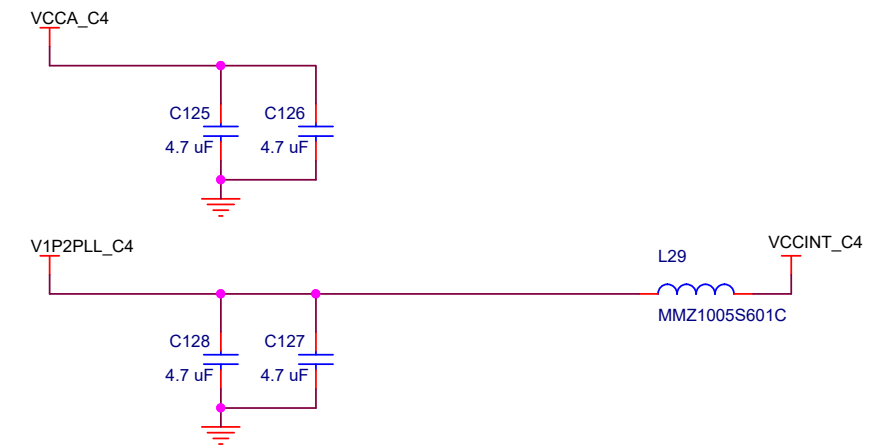
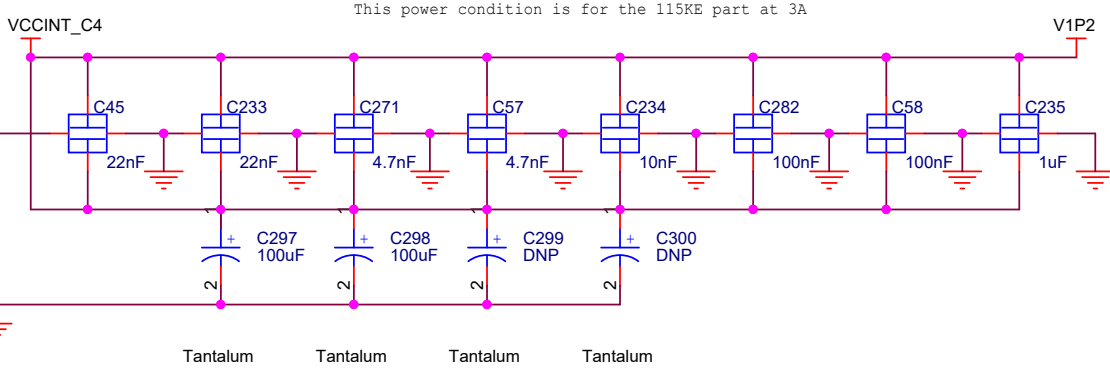
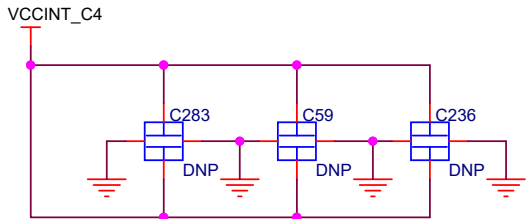
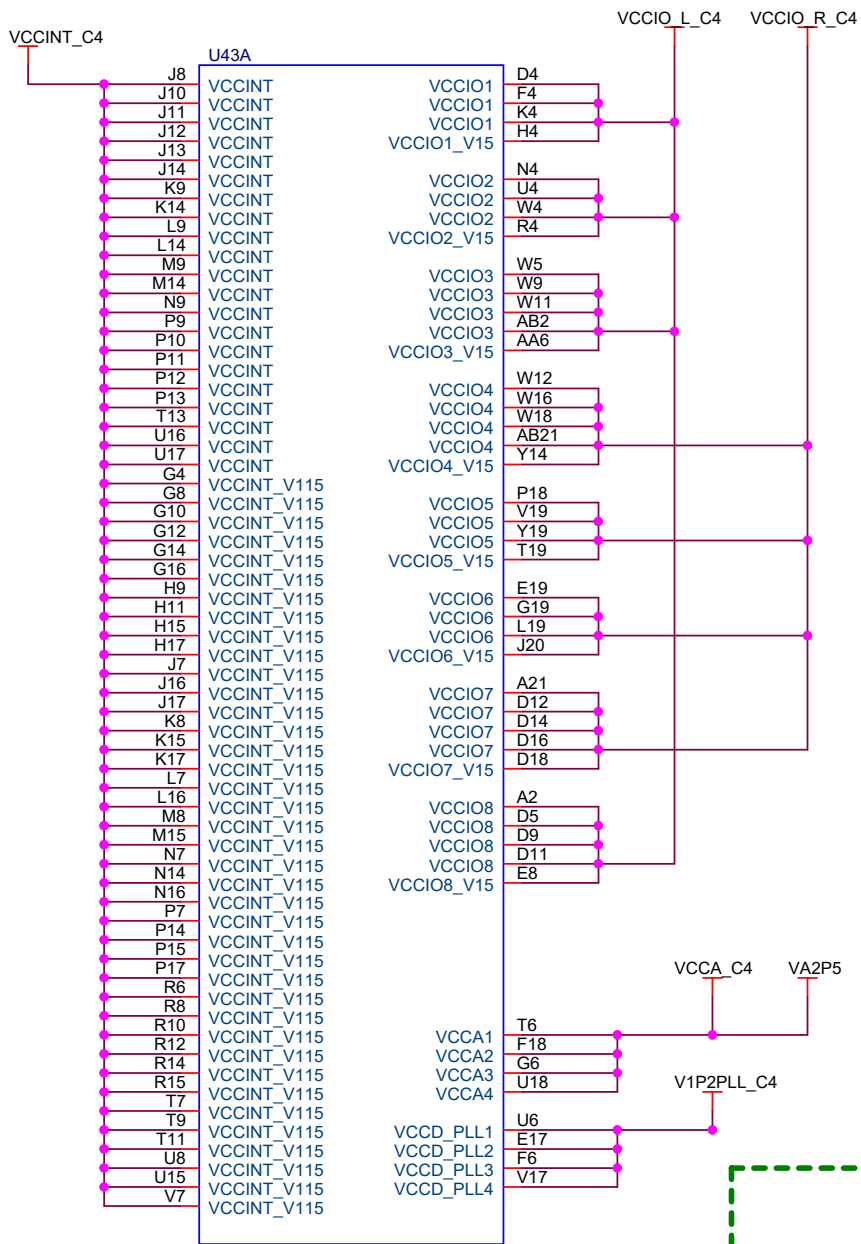


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VCCIO_L_C4 defines the "left" banks of the C4
 VCCIO_R_C4 defines the "right" banks of the C4
 The left side goes to the FX3, and the right side goes to the LMS.

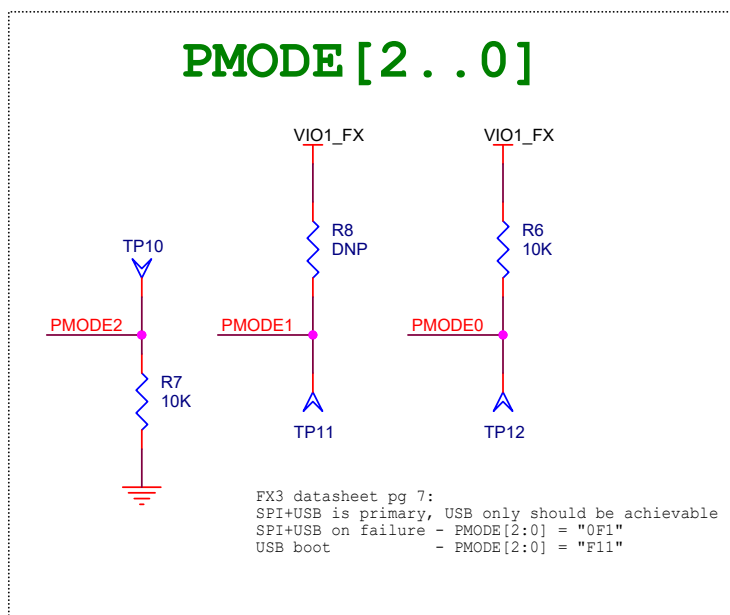
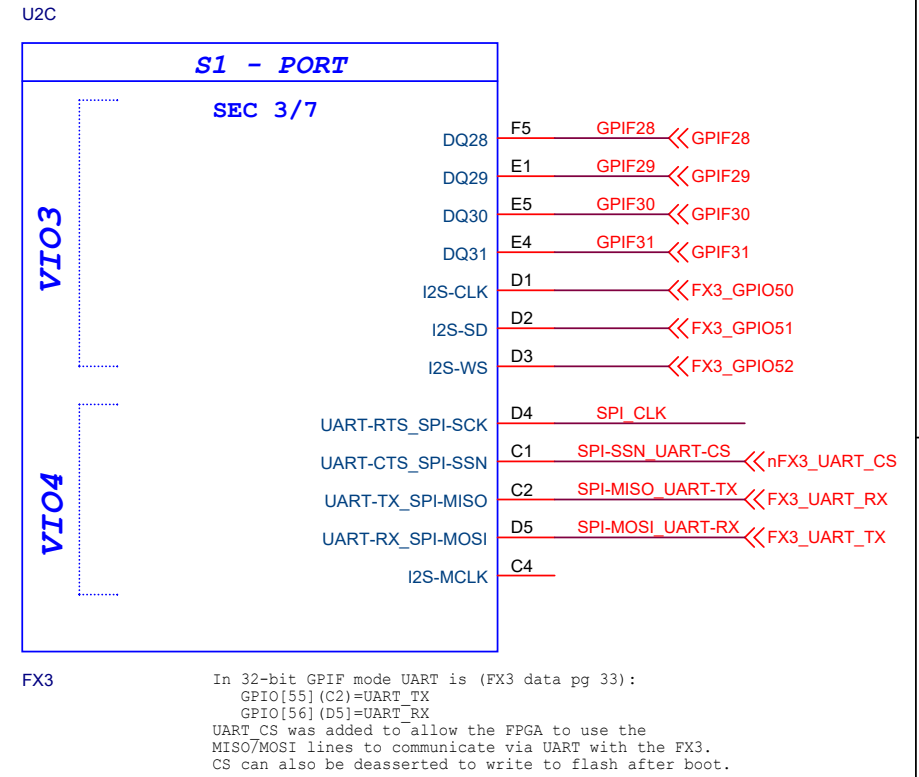
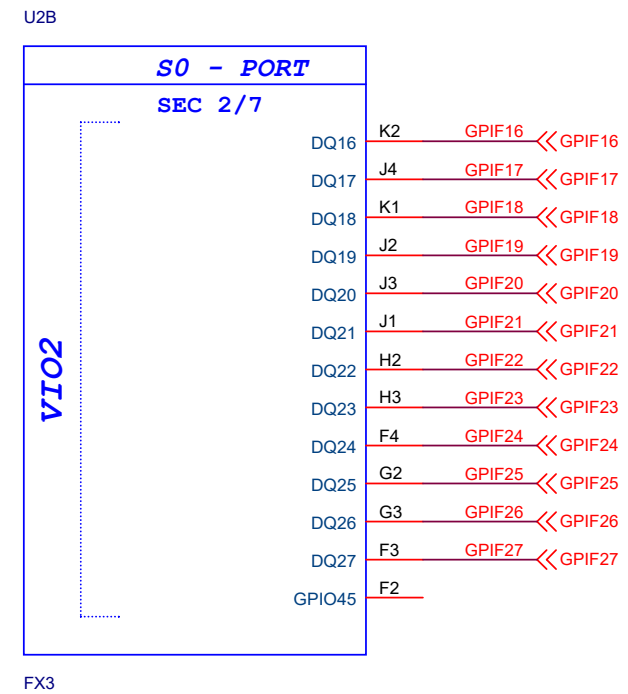
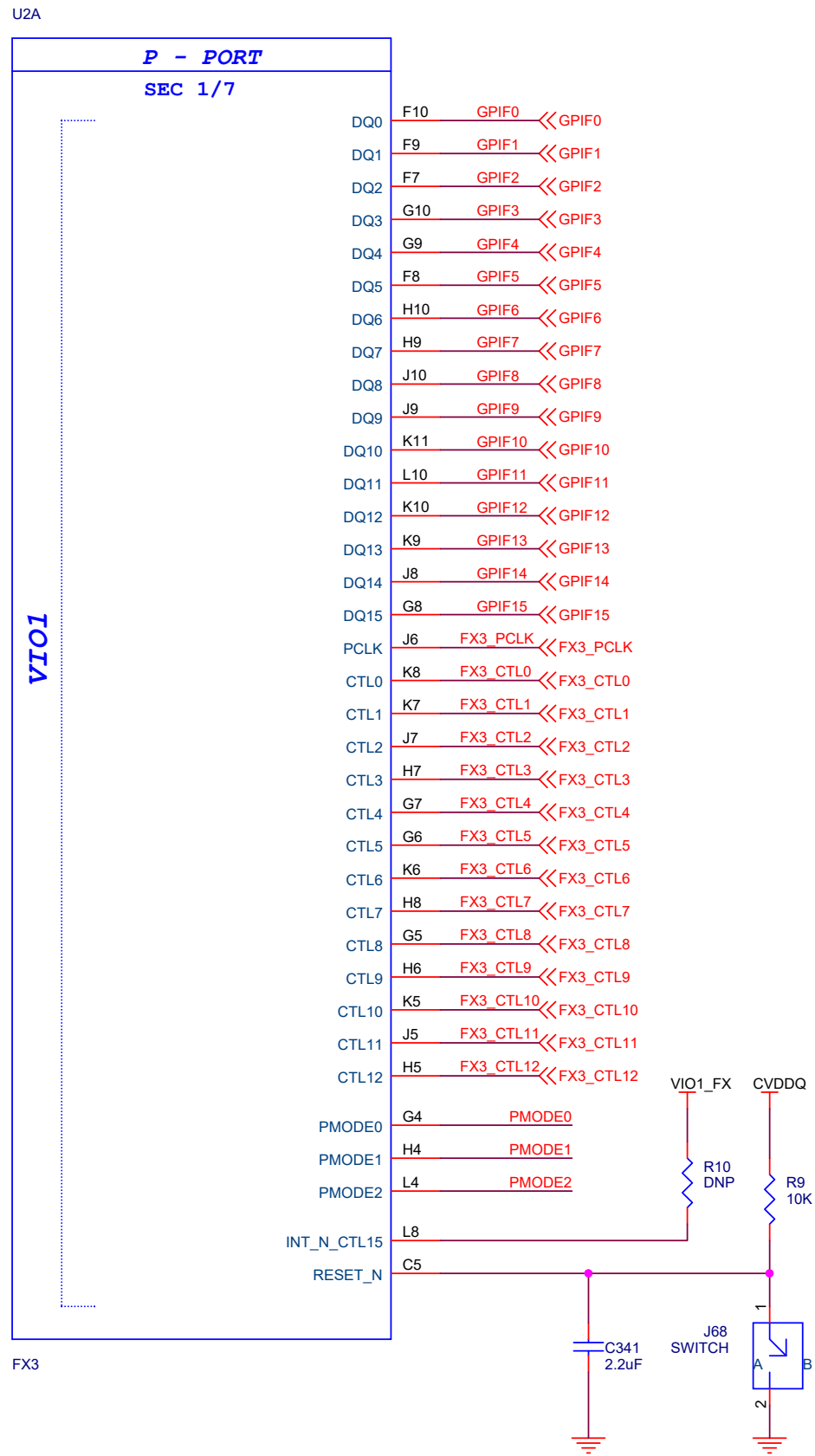
FPGA POWER

VCCINT @1.2V, MAX 3.1A
 VCCA2P5 @ 2.5, MAX 0.1A
 VCCIO @1.8V MAX 0.1A

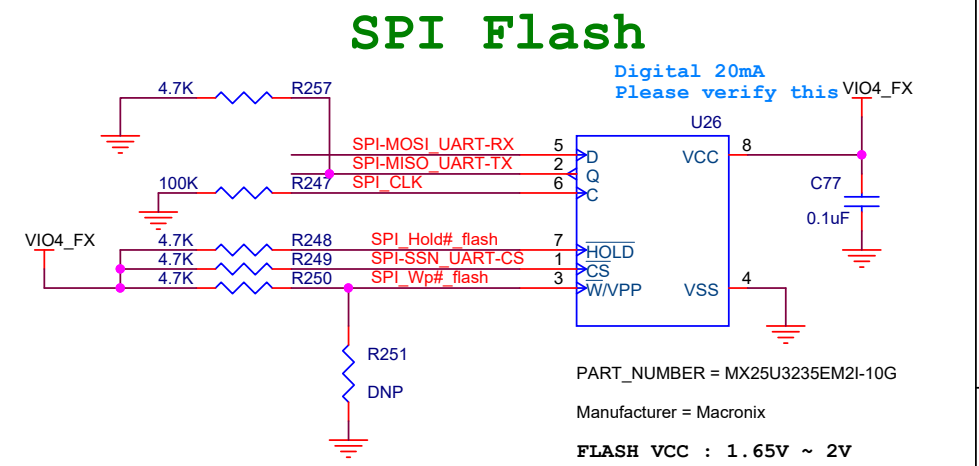


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FX3 GPIF + BOOT



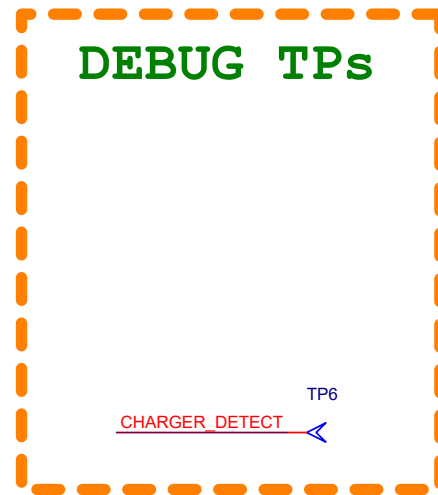
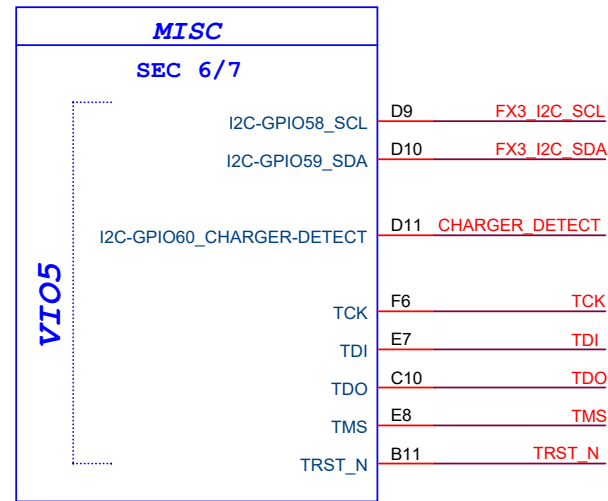
Add R257 so that SPI-boot works. C4's HIGH-Z state has a weak pull up, so it can be balanced out with a weak pull-down.



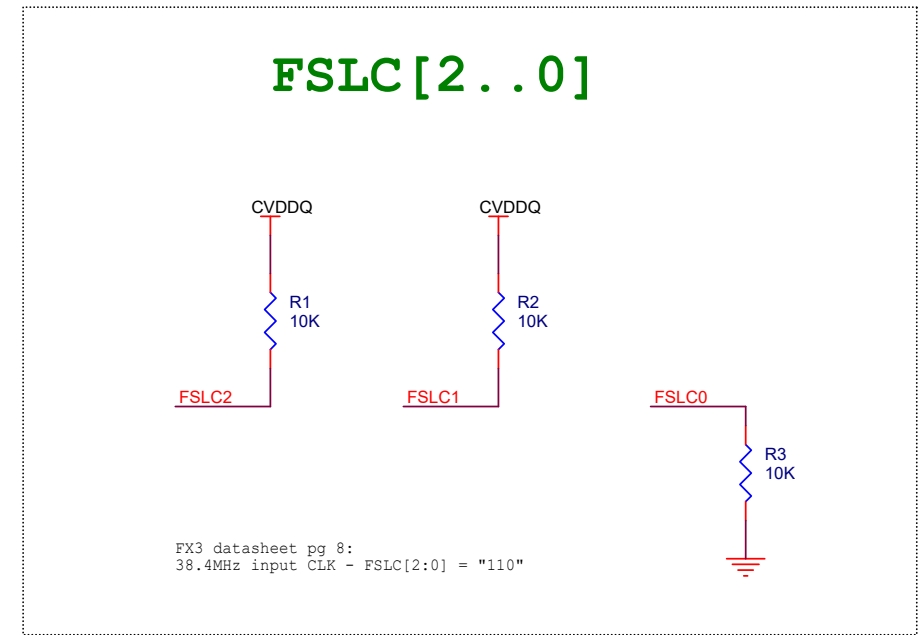
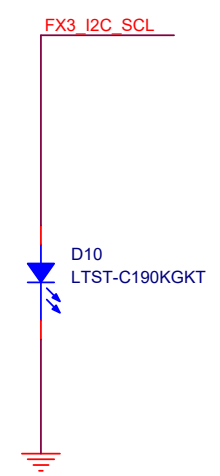
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FX3 DEBUG + CLOCK SEL

U2F

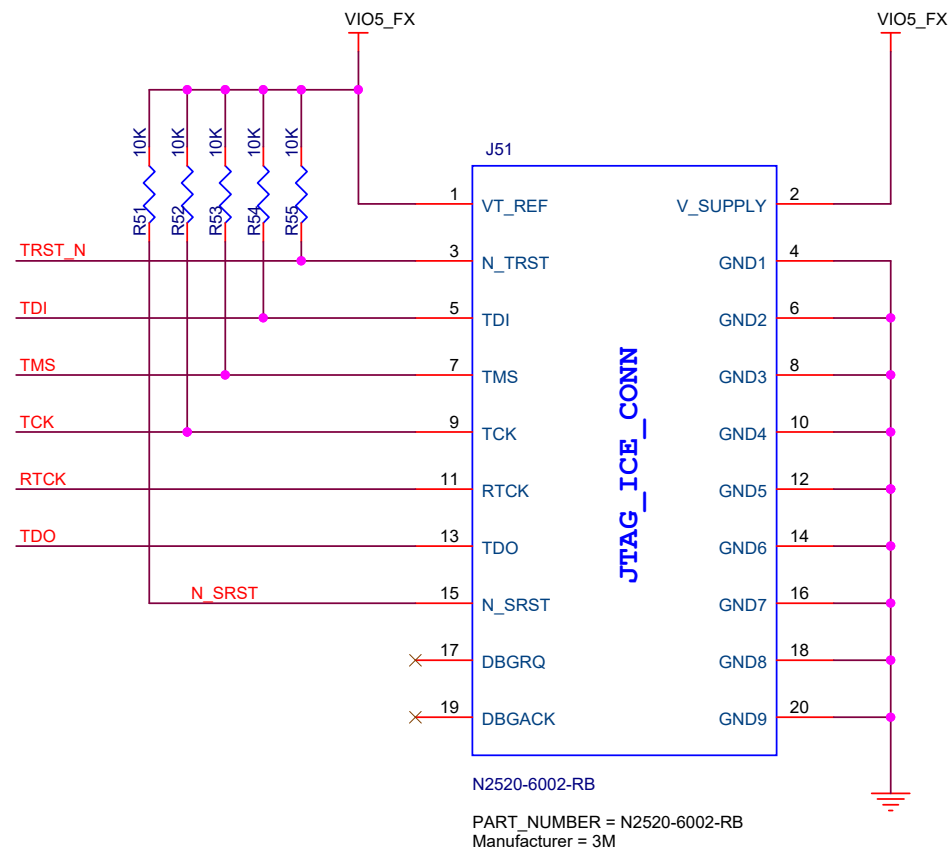


Debug LED

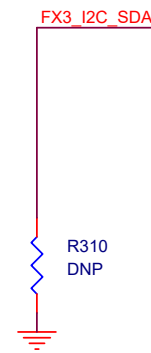


FX3

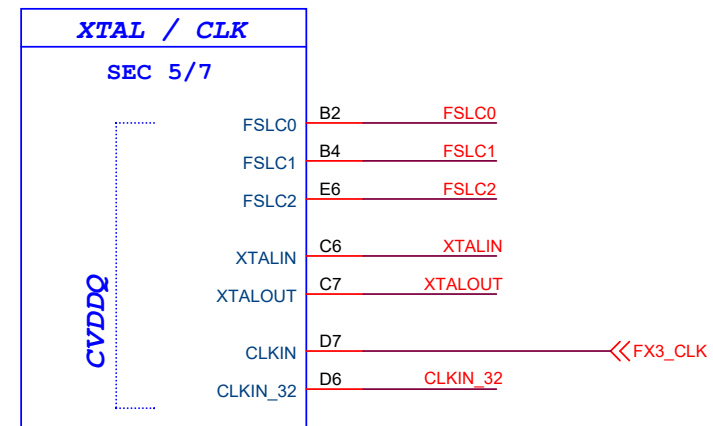
FX3 JTAG



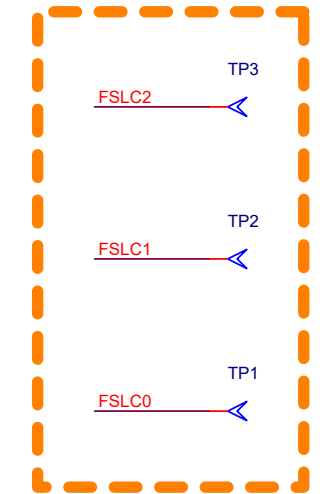
FPGA Version Resistor



U2E



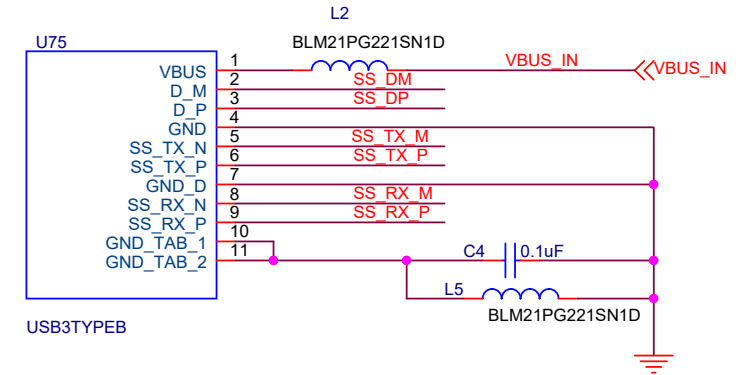
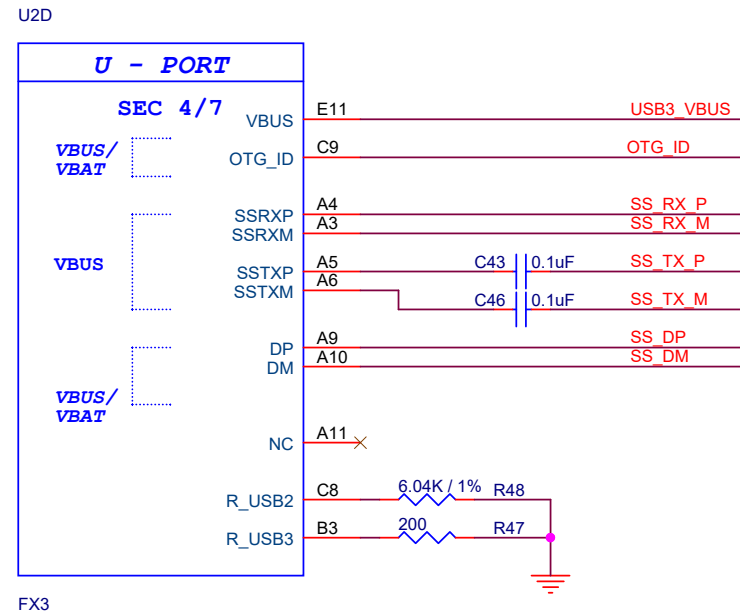
FX3



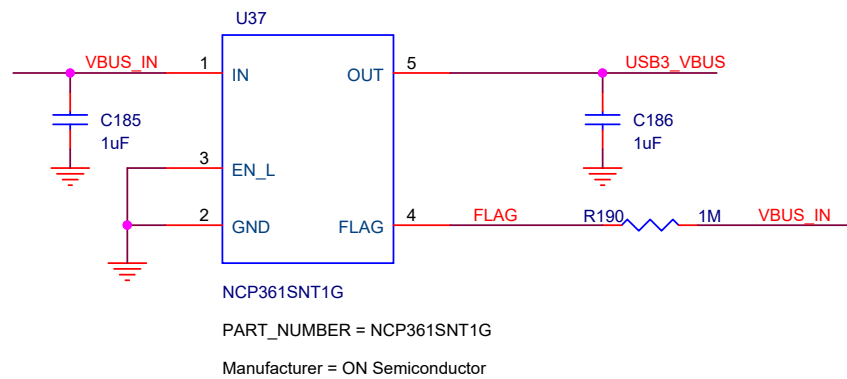
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USB CONNECTIONS

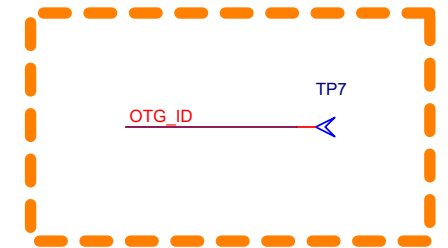
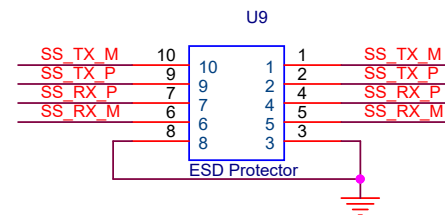
USB3.0 MICRO TYPE B



USB Positive Overvoltage Protection Controller



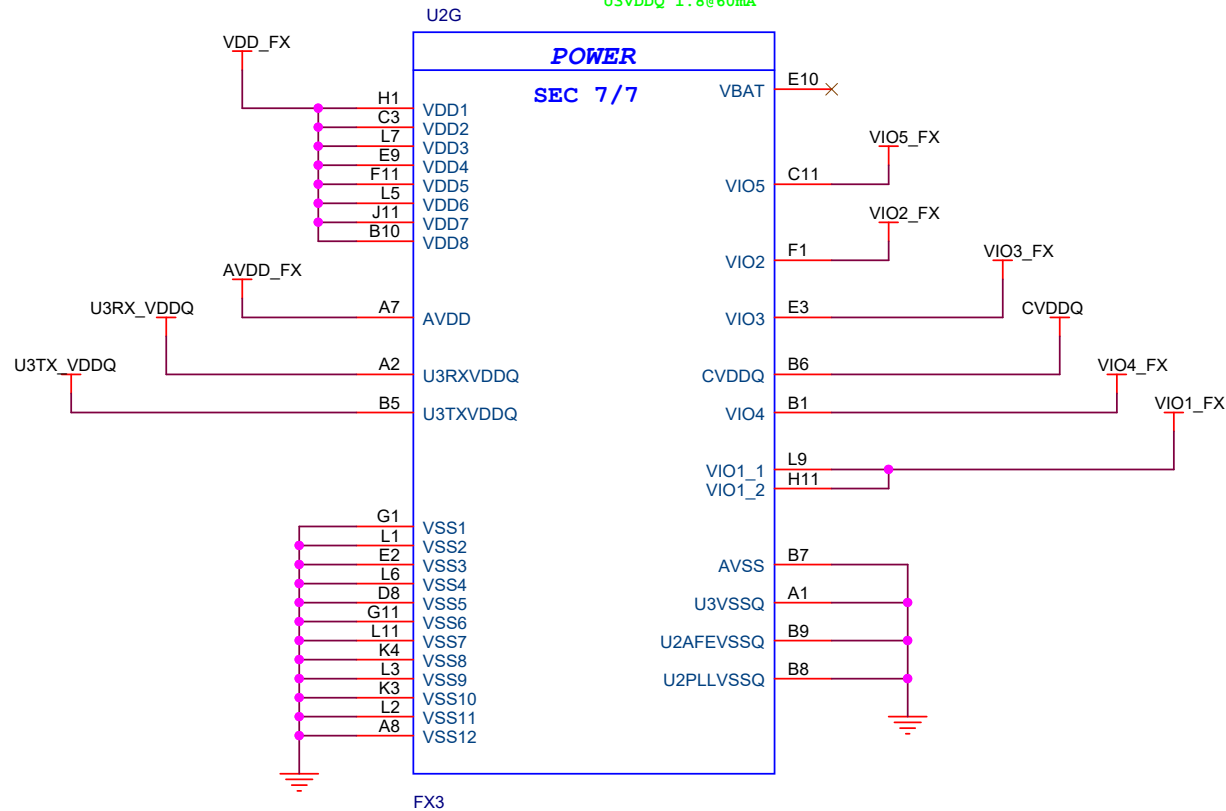
ESD DEVICE



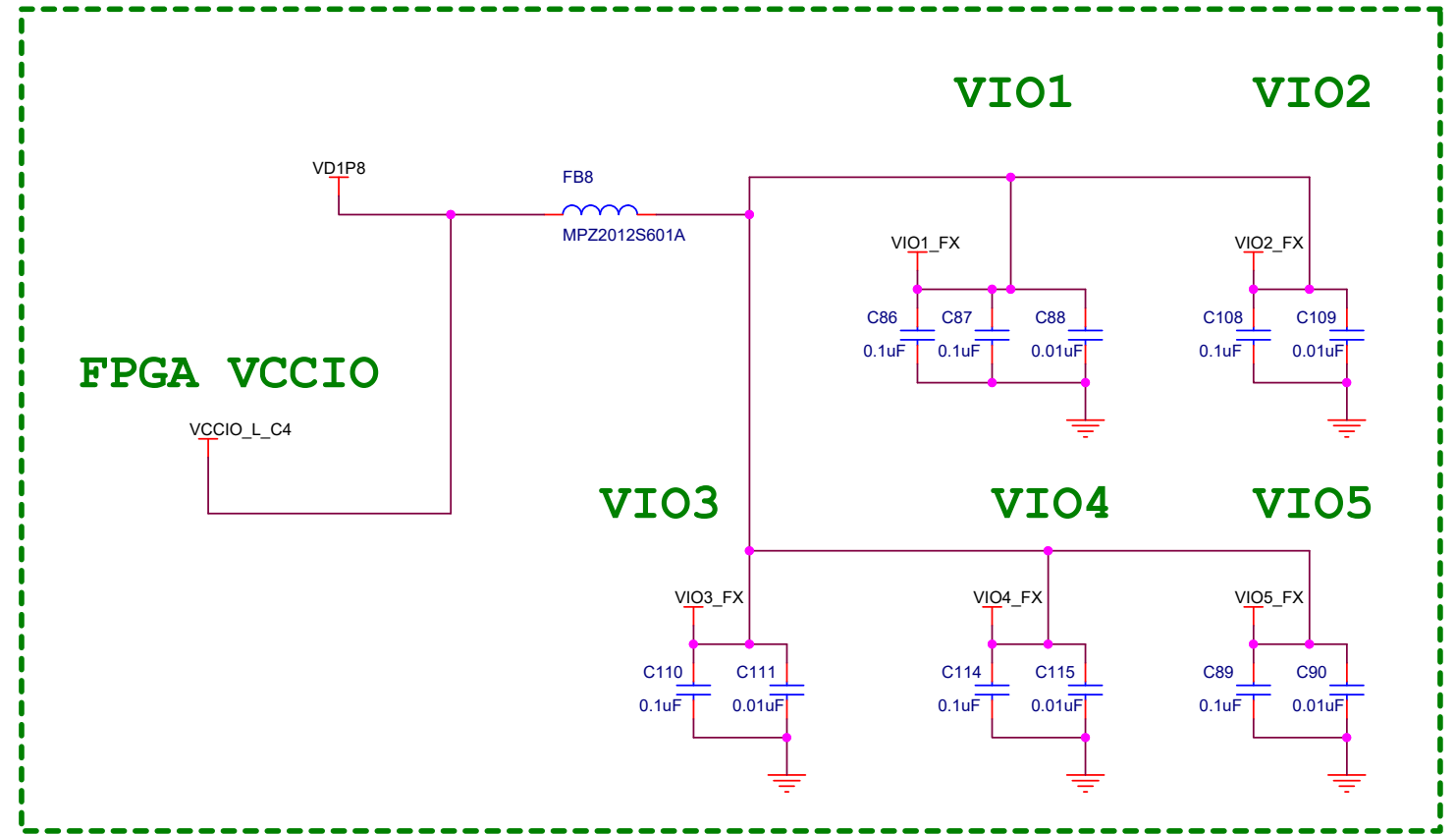
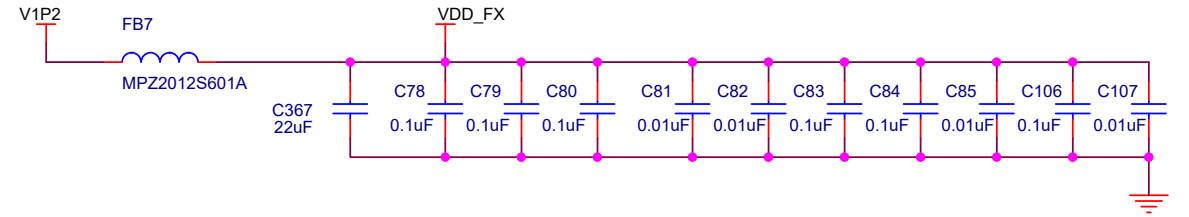
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FX3 POWER

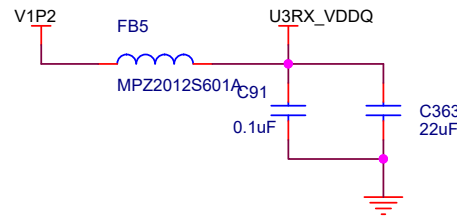
VDD+AVDD 1.2V@200mA
U3VDDQ 1.8@60mA



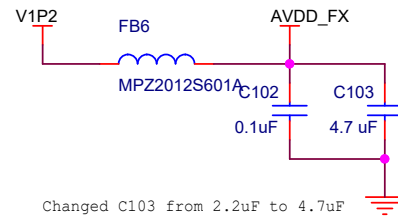
VDD



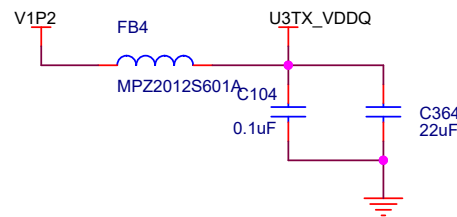
U3RX_VDDQ



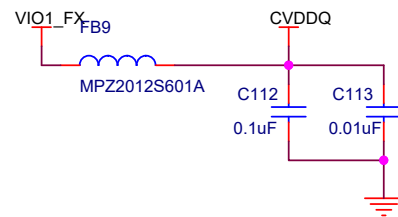
AVDD



U3TX_VDDQ



CVDDQ



- U3RX_VDDQ = V1P2
- U3TX_VDDQ = V1P2
- AVDD = V1P2
- CVDDQ = V1P8
- VDD = V1P2
- VIO1 = V1P8
- VIO2 = V1P8
- VIO3 = V1P8
- VIO4 = V1P8
- VIO5 = V1P8

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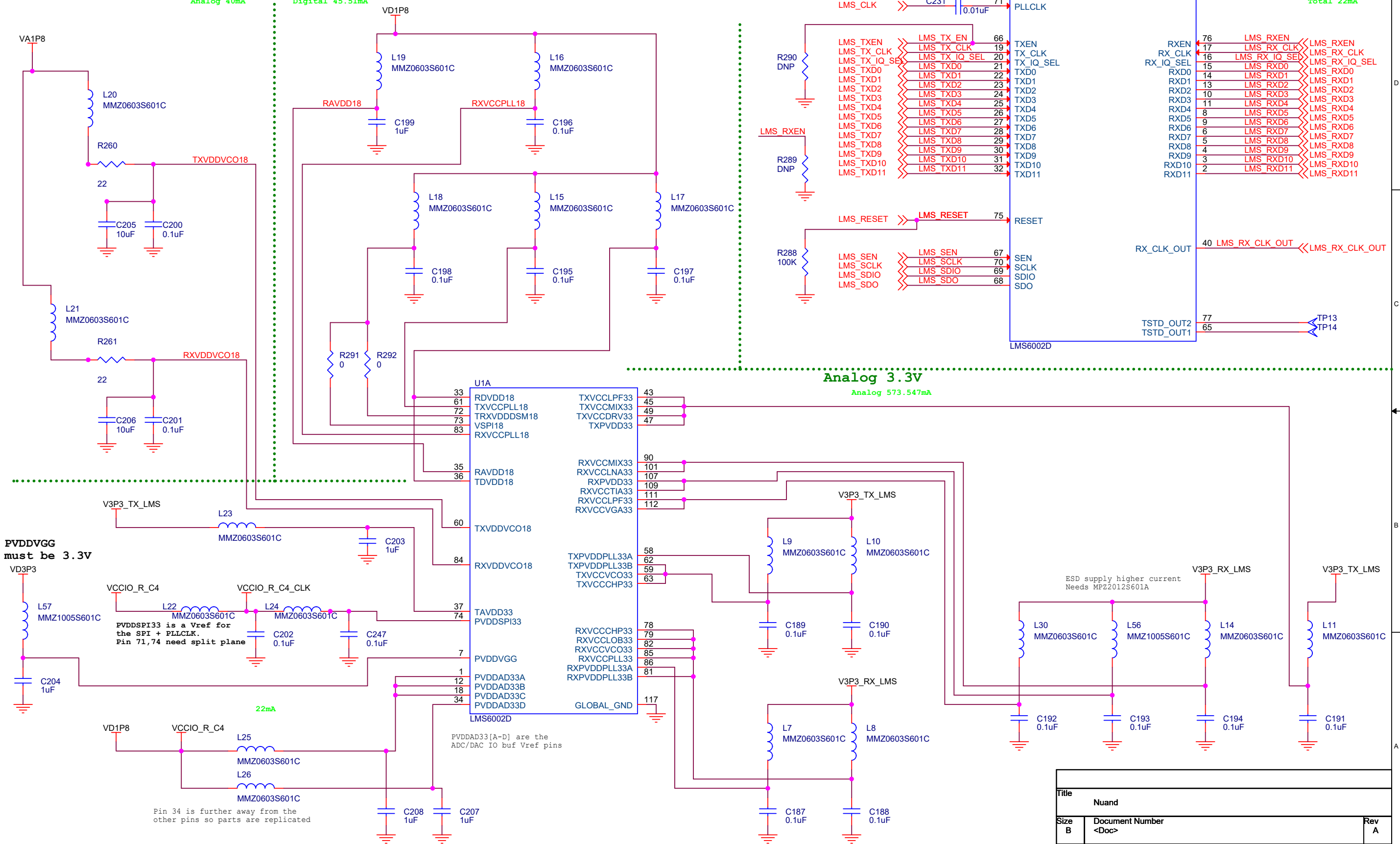
Analog 1.8V
Analog 40mA

Digital 1.8V
Digital 45.51mA

LMS DIGITAL

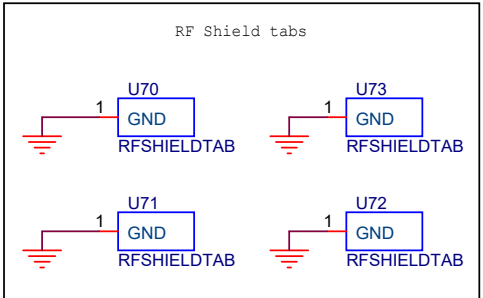
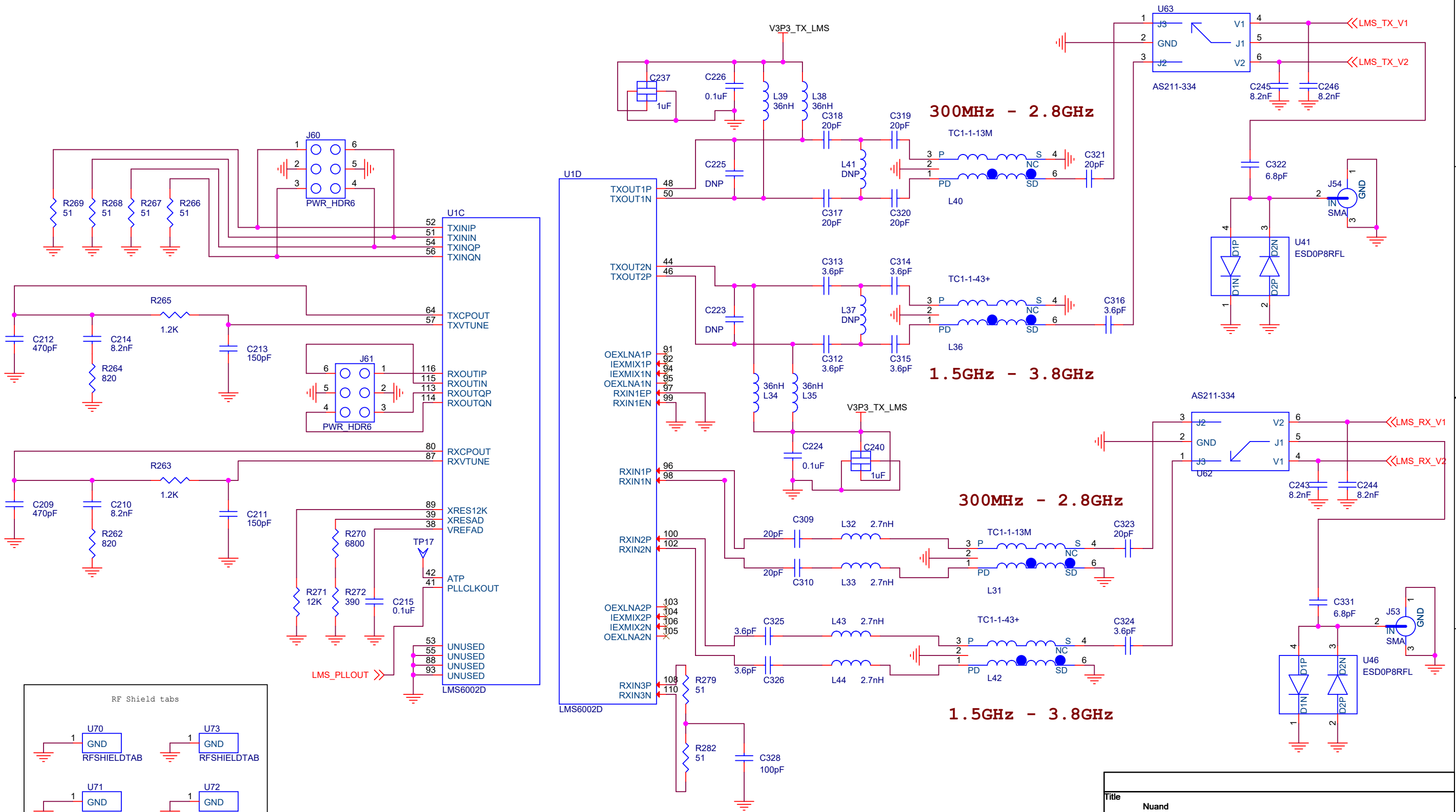
PLLCLK is Vref'd by PVDDSPI33

Digital 1.8V
Total 22mA



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LMS ANALOG + RF

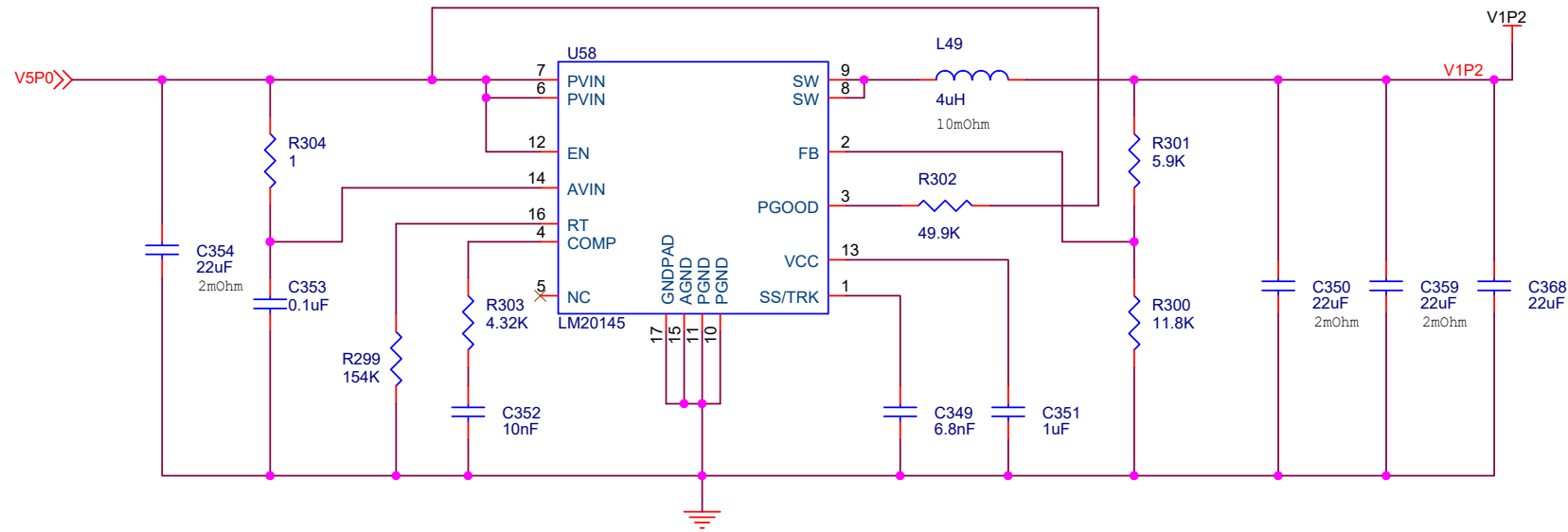


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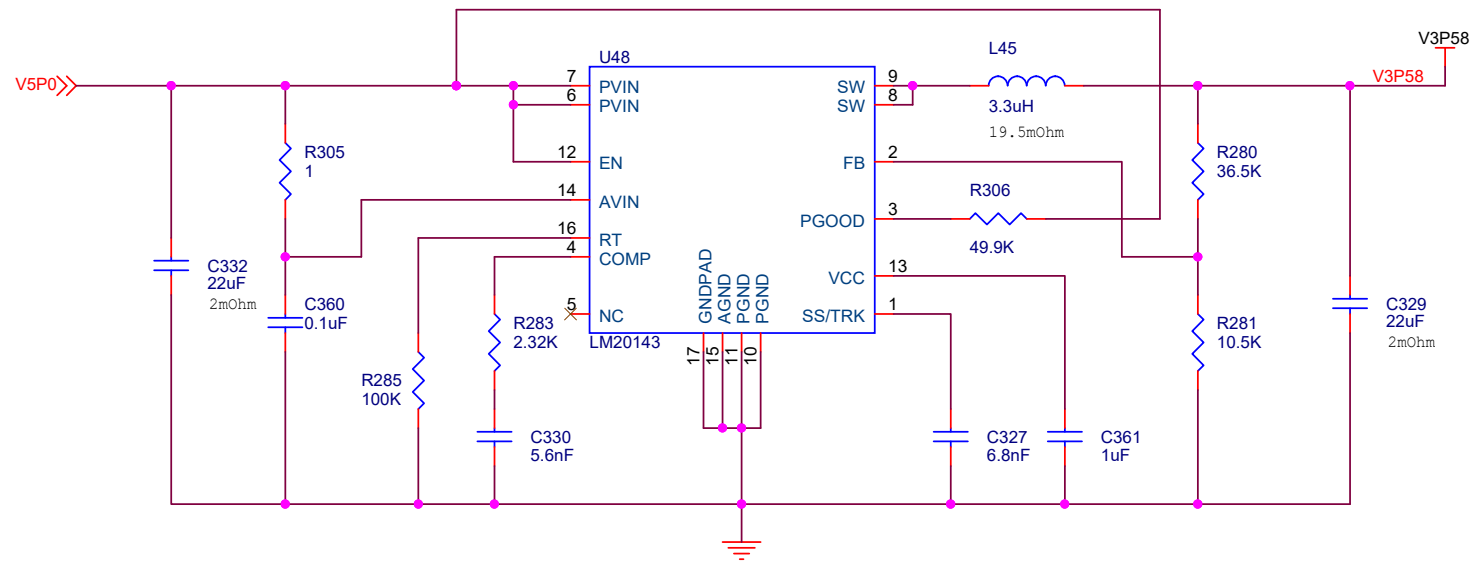
POWER DISTRIBUTION

The idea is to drop to 1.2V and 3.58V with SMPS.
Then drop to 3.3, 2.5, 1.8 from the 3.58V SMPS.

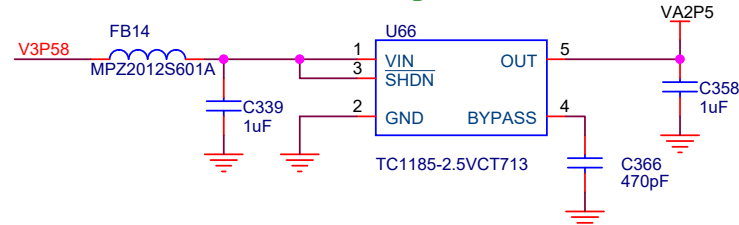
1.2V (min:200mA, typ:800mA) / 3100mA / 90% eff



3.58V ~800mA / 1300mA / 95% eff

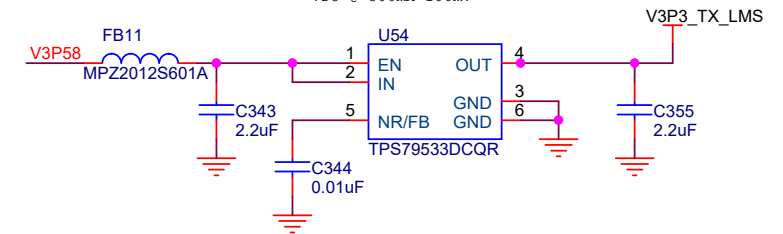


Analog 2.5V 30mA / 100mA



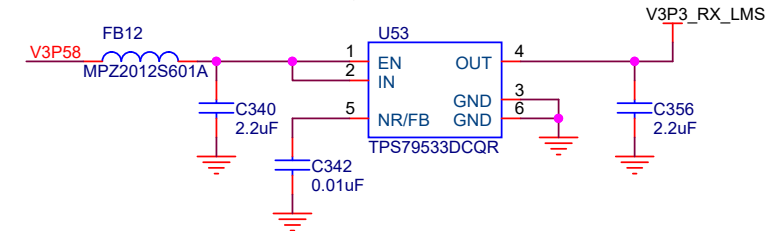
Analog 3.3V 280mA / 500mA

VDO @ 500mA 100mV



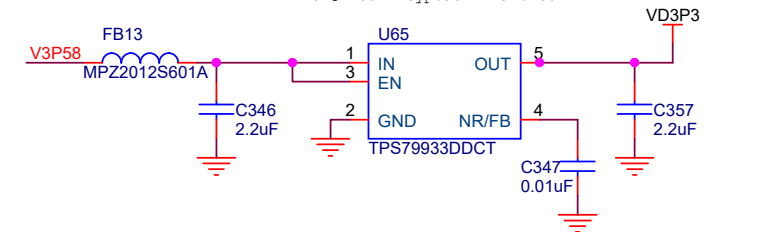
Analog 3.3V 220mA / 500mA

VDO @ 500mA 100mV



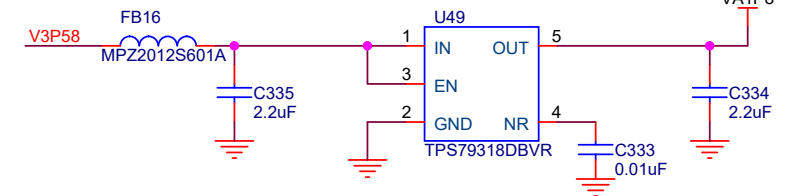
Digital 3.3V 106mA / 200mA

VDO @ 200mA typ:90mV max:160mV



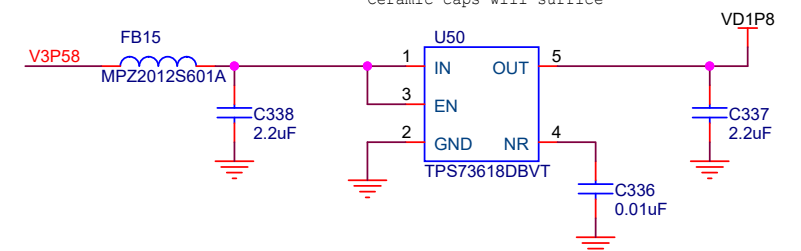
Analog 1.8V ~100mA / 200mA

Ceramic caps will suffice



Digital 1.8V 190mA / 400mA

Ceramic caps will suffice

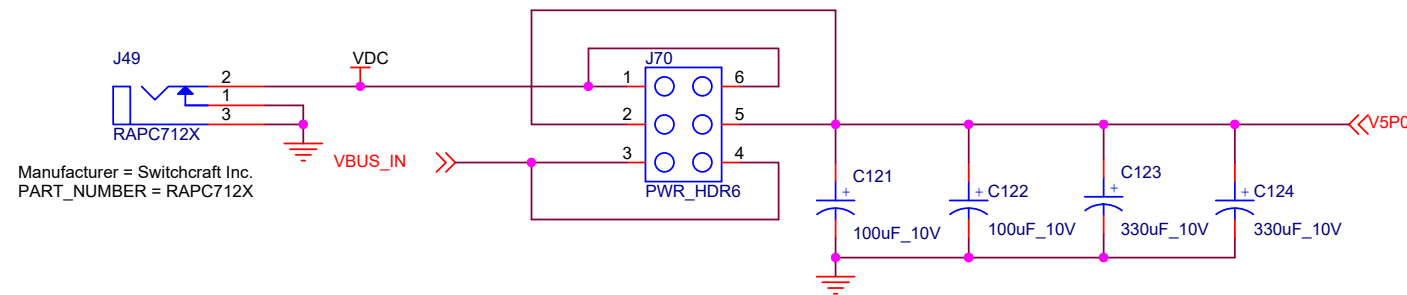


LMS - 67.1mA
FPGA - 25mA
FX3 - 25mA
Clocks - XOs - 20mA
SPI flash - 20mA max (verify this)

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POWER SELECTION + DEBUG

Jumpered power selection DC barrel vs USB3 bus



Scatter these testpoints throughout the design.
Testpoints will be PTH



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